The following claims listing sets forth the pending claims, and supercedes any previous listing.

1. (previously presented) An apparatus for improving reception in a receiver having N antennae, where N is an integer number with a value equal to or greater than 2, comprising:

N first receiver chips each associated with one of said antennae, each chip comprising a front-end section, equalizer, and a back-end section;

a digital combiner circuit for receiving signals from said first receiver chips, said digital combiner circuit comprising (N-1) first buffer memories, (N-1) second buffer memories, and a clock synchronizing module, with each buffer memory generating an output signal;

a common bus coupled to said first receiver chips and said digital combiner circuit;

said clock synchronizing module capable of generating a delay signal and aligning said output signal of each buffer memory based on a common clock;

said digital combiner circuit capable of generating a combined output signal; and

a single second receiver chip for receiving said combined output signal of said digital combiner circuit, said second receiver chip comprising a front-end section, equalizer and a back-end section.

2. (previously presented) The apparatus of claim 1 further comprising N tuners for receiving IF signals from each antenna and converting said IF signals to low IF signals before forwarding said low IF signals to said first receiver chips.

3. (previously presented) The apparatus of claim 2 further comprising N analog to digital converters, each receiving said low IF signal and generating a digital input signal to be forwarded to said first receiver chips.

4. (original) The apparatus of claim 3 wherein each of said first receiver chips generates an equalizer output signal in response to said digital input signal, wherein said digital input signal is processed in said front end section and said equalizer, said equalizer then generating an equalizer output signal.

5. (previously presented) The apparatus of claim 4 wherein each said (N-1) first buffer memories and each said (N-1)second buffer memories receive said equalizer output signal and generate a synchronized memory buffer output signal, said synchronized memory buffer output signal being weighted based on signal quality indicator value.

6. (original) The apparatus of claim 5, wherein said signal quality indicator value is passed through said common bus, said common bus being controlled by a computer.

7. (original) The apparatus of claim 5, wherein said synchronized memory buffer output is weighted using a maximum ratio combining algorithm.

8. (original) The apparatus of claim 5, wherein said digital combiner circuit further comprises an adder, said adder producing said combined output signal in response to said weighted synchronized memory buffer output signals.

9. (original) The apparatus of claim 1, wherein said second receiver chip receives said combined output signal at said back end section.

10. (original) The apparatus of claim 1, wherein said digital combiner circuit is an FPGA.

11. (previously presented) The apparatus of claim 1, wherein each of said (N-1)first buffer memories is a FIFO.

12. (previously presented) The apparatus of claim 1, wherein each of said (N-1)second buffer memories is a RAM.

13. (original) An apparatus for improving signal reception in a signal receiver having a first antenna and a second antenna coupled to a first tuner and a second tuner respectively, said first tuner passing a first channel low IF signal into a first analog to digital converter and said second tuner passing a

second channel low IF signal into a second analog to digital converter, said analog to digital converters producing digital output signals, said apparatus comprising:

a first receiver chip and a second receiver chip, each coupled to said first and second analog to digital converters respectively, each of said first and second receiver chips comprising a front end section, equalizer and a back end section, wherein said digital output signal from each of said first and second analog to digital converters is passed through said front-end section and said equalizer of each of said first and second receiver chips, said equalizers producing equalizer output signals;

a digital combiner circuit for receiving said equalizer output signals from said first and second receiver chips, said digital combiner circuit comprising:

a first buffer memory for receiving said first equalizer output and a first clock signal from said first receiver chip,

a second buffer memory capable of receiving said second equalizer output and a second clock signal from said second receiver chip,

a clock synchronizing module for generating a delay signal and aligning said first and second output signals from said first and second buffer memories based on a common clock, said delay signal utilized as an input signal into said first buffer memory;

said digital combiner circuit is capable of generating a combined output signal;

a third receiver chip for receiving from said digital combiner circuit, said third receiver chip comprising a front-end section, equalizer and a back-end section, wherein said third receiver chip receives said combined output signal at said back-end section;

a common bus coupled to said first and second tuners, to said first and second receiver chips and to said digital combiner circuit.

14. (original) The apparatus of claim 13, wherein said digital combiner circuit is an FPGA.

15. (original) The apparatus of claim 13, wherein said first buffer memory is a FIFO.

16. (original) The apparatus of claim 13, wherein said second buffer memory is a RAM.

17. (original) The apparatus of claim 13, further comprising an adder for combining weighted outputs of said first and second buffer memories, said adder generating said combined output signal.

18. (original) The apparatus of claim 17, wherein said outputs of said first and second buffer memories are weighted based on a weighting factor, said weighting factor is determined from a signal quality indicator value by utilizing a maximum ratio combining algorithm.

19. (previously presented) A method for improving signal reception in a signal receiver having a first antenna and a second antenna comprising the steps of:

programming a common bus to enable first and second tuners to operate on a same channel;

down-converting first and second IF signals received from said first and second antennae to a first low IF signal and to a second low IF signal respectively;

converting said first and second low IF signals to said first and second digital signals;

modifying said first and second digital signals in a front-end section and an equalizer of a first and second receiver chips to recover timing and to correct distortions in said first and second digital signals;

routing said first and second digital signals to a digital combiner circuit;

delaying said first and second digital signals in a first memory buffer and a second memory buffer based on a delay signal generated by clock synchronizing means;

aligning said first and second digital signals to a common clock;

weighting said first and second digital signals based on a signal quality indicator value;

adding said weighted digital signals;

passing a combined output signal into a back-end section of a third receiver chip;

20. (original) The method of claim 19, wherein said digital signals are weighted using a maximum ratio combining algorithm.

21. (previously presented) A method for improving reception in a receiver having N antennae, where N is an integer number that is greater than or equal to 2, comprising the steps of:

receiving N signals from each respective N antennae in first receiver chips;

processing the signals in a digital combiner circuit that includes N buffer memories and a clock synchronizing module, in order to generate a delay signal that synchronizes and combines output signals from the N buffer memories to generate a combined output signal; and

feeding the combined output signal to a single second receiver chip.